

## IN THE CLAIMS

Following is a complete set of claims as amended with this response, which includes an amendment to claim 3.

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1           1.     (canceled)

1           2.     (previously amended) The method of claim 3, further comprising selecting said  
2 memory banks for access by one of the first and second processors.

1           3.     (currently amended) A method for allocating real-time audio data from a plurality  
2 of audio channels in a system having a first processor and a second processor, the method  
3 comprising:

4                 providing a plurality of memory banks of semiconductor memory devices, each memory  
5 bank being accessible to the first and second processors for operations selected from the group  
6 comprising read and write operations, the ~~second~~ plurality of memory banks includes two  
7 memory banks; and

8                 storing subsets of said audio data in the ~~second~~ plurality of memory banks, the subsets  
9 corresponding to different groups of audio channels.

1           4.     (original)The method of claim 3 wherein one subset of said audio data  
2 corresponds to even-numbered audio channels and one other subset of said audio data  
3 corresponds to odd-numbered audio channels.

1           5.     (canceled)

1           6.     (previously amended) A system having first and second buses for processing real-  
2 time audio data from a plurality of audio channels, the system comprising:

3                 a first processor and a second processor coupled to said first and second busses,  
4 respectively;

5                 a plurality of memory banks of semiconductor memory devices coupled to said first and  
6 second buses for storing said audio data, said plurality of memory banks being accessible to the

7 first and second processors for operations selected from the group comprising read and write  
8 operations, said plurality of memory banks storing subsets of audio data, said subsets  
9 corresponding to different groups of audio channels; and  
10 a plurality of selectors coupled said first and second buses to select said memory banks  
11 for access by one of said first and second processors.

1 7. (previously amended) The system of claim 6 wherein the plurality of selectors  
2 include a plurality of address multiplexers and data transceivers.

1 8. (previously amended) The system of claim 6 wherein one subset of said audio  
2 data corresponds to even-numbered audio channels and one other subset of said audio data  
3 corresponds to odd-numbered audio channels.

*F*  
*Cont* 1 9. (previously amended) The system of claim 6, wherein the memory banks include  
2 dynamic random access memories.

1 10. (previously amended) The method of claim 3, wherein storing further comprises  
2 interleaving the subsets of data.

1 11. (previously amended) The system of claim 6, wherein the subsets are stored in the  
2 memory banks in an interleaving manner.

1 12. (previously amended) The method of claim 3, wherein storing comprises storing  
2 one of the subsets of audio data in one of the memory banks, said method further comprising  
3 reading stored audio data from a second of the memory banks.

1 13. (previously amended) The method of claim 3, wherein the first processor  
2 performs a read operation on a first memory bank of the plurality of memory banks and the  
3 second processor performs a write operation on a second memory bank of the plurality of  
4 memory banks.

1 14. (previously amended) The system of claim 6, wherein subsets of audio data are  
2 stored in one of the memory banks and stored audio data is read from a second memory bank of  
3 the memory banks.

F  
cont 1 15. (previously amended) The system of claim 6, wherein the first processor performs  
2 a read operation on a first memory bank of the plurality of memory banks and the second  
3 processor performs a write operation on a second memory bank of the plurality of memory banks.

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